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(56) Documents Cited
EP 0519393 A US 5268333 A

(58) Field of Search
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(54) **Method for planarization of semicondoctor device**

(57) In a method for planarizing a semiconductor device, an interlevel insulating layer 17, e.g. of silicon dioxide, and a layer for the planarization 18, e.g. of BPSG, containing dopants therein are formed on a semiconductor substrate. The dopants are diffused out of the layer 18 by a first thermal annealing step. Afterwards, the layer 18 is flowed by a second thermal annealing step, and thermal oxide is formed thereon as a passivation layer (19). Such a method avoids precipitation of the dopants after annealing.

FIG.2C

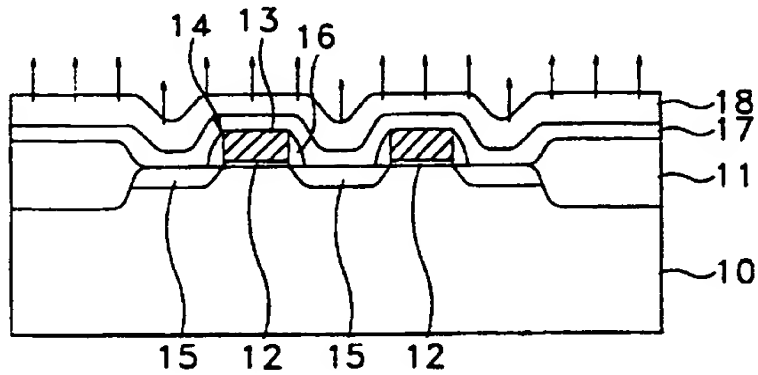


FIG. 1
PRIOR ART

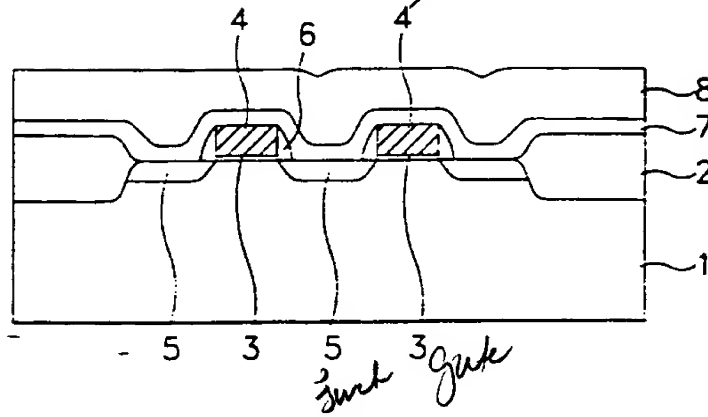


FIG. 2A

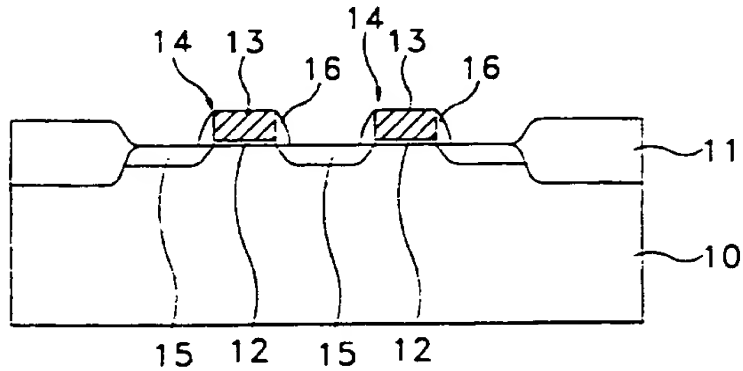


FIG. 2B

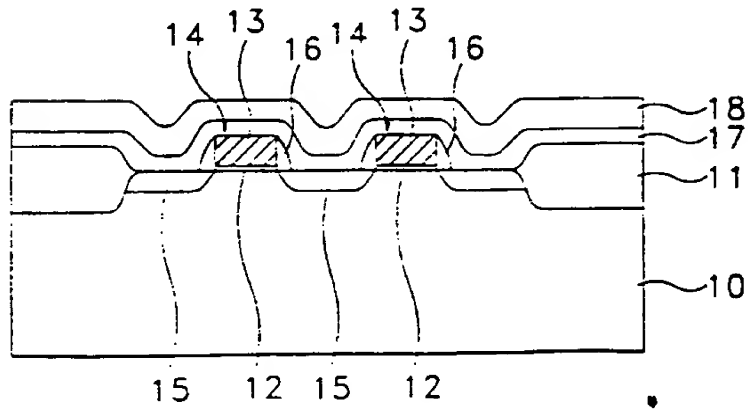


FIG.2C

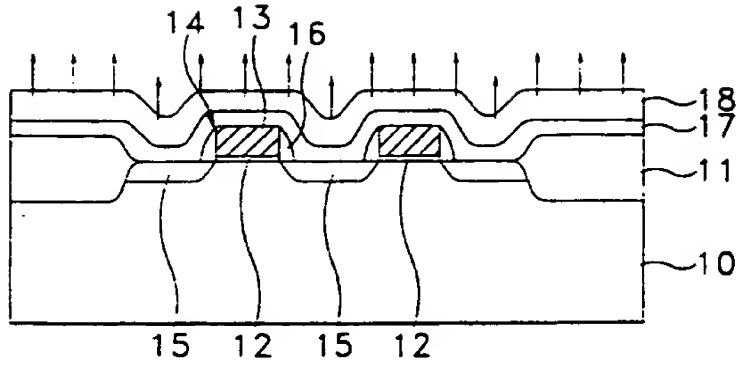


FIG.2D

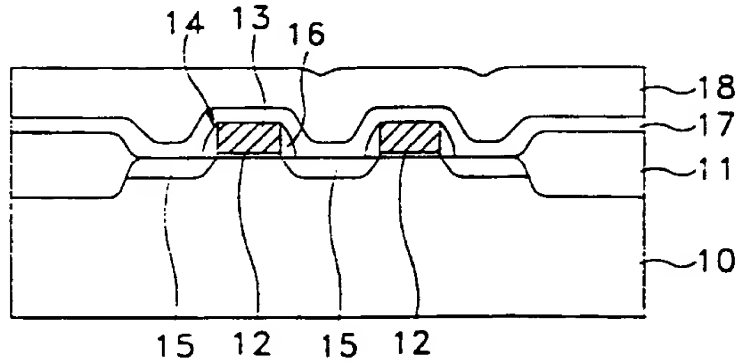
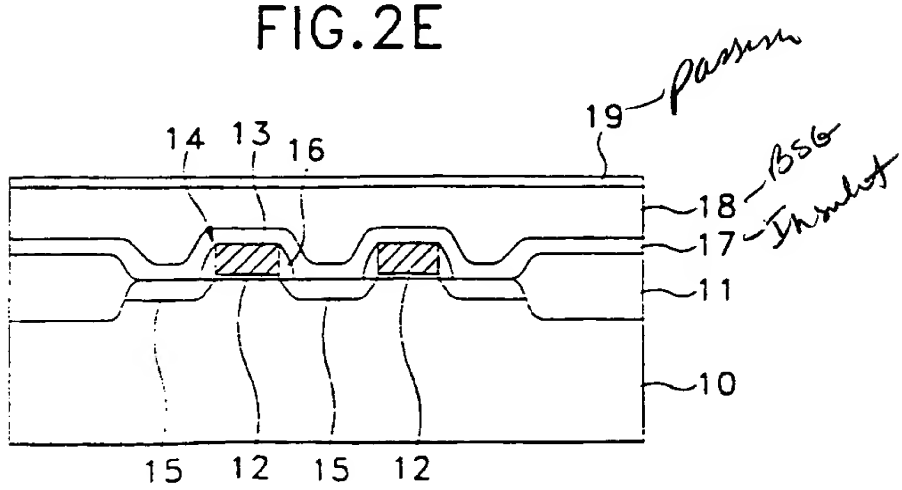


FIG.2E



METHOD FOR PLANARIZATION OF SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to a method for the planarization of a semiconductor device, and more particularly to a method capable of preventing dopants from precipitating during the flow process of the deposited layer for the planarization.

Description of the Related Art

In the semiconductor devices, active devices such as transistors, passive devices such as resistors, and a multilayer interconnection structure on the substrate are required. In the formation of the active device and passive device, the substrate surface can become uneven. Due to the high densification and high integration of the semiconductor device in recent years, the unevenness of the substrate surface has become conspicuous, and therefore more of a problem. It becomes more difficult to form a highly precise fine pattern. In addition short of the interconnection and the like are also liable to occur. To solve these problems the technique for flattening the substrate surface is required.

Conventionally, a layer of insulating material such as silicon oxide is applied over such uneven surfaces, to permit the formation of a more finely patterned layer onto the surface of a

non-planarized layer. This silicon dioxide layer, however, tends to conform to the underlying topography resulting in the creation of a non-planar or stepped surface. Accordingly, it is very difficult to form the more finely patterned layer on the uneven surface using a general lithography process.

Thus, there provided a glass material such as spin on glass (SOG), and a material containing boron and/or phosphorous such as borophosphosilicate glass(BPSG), phosphosilicate glass(PSG) and borosilicate glass(BSG) to be used for the formation of a planarized layer.

Among these layers for the planarization, a BPSG layer having boron concentration at 3-5 w% and phosphorous concentration at 3-5 wt% is deposited on the substrate having the semiconductor devices at a low temperature of 400-450°C. Then, a thermal flow process is performed at a temperature of 800-850°C, immediately following the deposition whereby a planarized surface is obtained. At this time, as boron concentration in BPSG increases, the flow temperature decreases. The degree of the planarizationare also proportional to boron and phosphorous concentrations. In addition, BPSG plays role in removing the topology existing, for example, between a gate electrode and a first metal interconnection.

Referring to Fig. 1, a method for the planarization between a gate electrode and a first metal interconnection using BPSG according to the conventional art, is described.

A gate oxide film 3, a gate electrode 4, and junction regions 5 are formed in and on a silicon wafer 1 with field oxide 2 for the

isolation of a device using a conventional method. Afterwards, sidewall spacer 6 are formed at both sides of the gate electrode 4 and then an inter-level insulating layer 7 such as silicon dioxide is formed on the silicon wafer 1 by a chemical vapor deposition(CVD) method. Next, in order to even the overall surface topology due to the field oxide 2 and the gate electrode 4, a BPSG layer 8 is formed on the inter-level insulating layer 7 by either plasma enhanced chemical vapor deposition(PECVD) or atmospheric pressure chemical vapor deposition(APCVD). As described above, it is preferable that the concentration of boron and phosphorous contained in BPSG layer 8 be 3.5-5.0 wt% to achieve a more planar surface.

The wafer 1 on which BPSG layer 8 is formed, is loaded to a diffusion furnace maintaining atmospheric pressure and a temperature of 750-850°C. Afterwards, the temperature of the diffusion furnace is elevated to 800-850°C, and nitrogen(N2) gas is supplied to the diffusion furnace. Under the above-mentioned conditions, thermal annealing process for the flow of the deposited BPSG layer 8, proceeds for 20-60 minutes, whereby BPSG layer 8 is planarized. Lastly, the temperature of the diffusion furnace lowers to 650-800°C, and the wafer 1 is unloaded from the diffusion furnace.

Not shown in Fig. 1, a second insulating layer is then formed on the planarized BPSG layer of the wafer 1, and predetermined portions of second insulating layer, BPSG layer, and first insulating layer are etched to expose the underlying junction

regions, thereby forming contact holes. Afterwards, metal interconnects are formed to electrically contact with junction regions.

Then, boron and phosphorous atoms doped in BPSG layer 8 diffuse outwards from the surface during the flow process because of the high flow temperature. Due to the above-mentioned facts, diffused boron and phosphorous atoms are gathered to the surface of BPSG layer 8, and thereby the surface thereof becomes over-saturated. Afterwards, when the wafer 1 is unloaded to the outside, the atoms gathered at the surface of the BPSG layer 8 is precipitated to crystal from the abrupt change on the surface temperature, and from the moisture present the atmosphere. These precipitated crystals generate not only crystal defects on the formation of a pattern but also pattern defects such as notching. Moreover, it degrades the insulating property of BPSG layer 8.

SUMMARY OF THE INVENTION

Accordingly, it is one object of the present invention to provide a method for the planarization of a semiconductor device capable of preventing the generation of crystal defects by preventing dopants contained in BPSG layer for the planarization from precipitating when a wafer, on which the BPSG layer is formed, is unloaded from a diffusion furnace after the flow process of the deposited BPSG layer has been completed.

Another object of this invention is to provide a method for

the planarization of a semiconductor device capable of facilitating the patterning of a layer that is deposited on BPSG layer.

According to the present invention, a method for the planarization of a semiconductor device comprises the steps of: providing a semiconductor substrate on which a patterned layer having a topology is formed; forming an inter-level insulating layer on the semiconductor substrate; forming a layer for the planarization containing a dopant on the inter-level insulating layer; diffusing the dopant contained in the layer for the planarization outward from the surface; and flowing the layer for the planarization.

BRIEF DESCRIPTION OF THE DRAWINGS

Further objects and advantages of the present invention will be apparent from the following description, reference being had to the accompanying drawings wherein preferred embodiment of the present invention are clearly shown.

In the drawings:

Fig. 1 is a cross-sectional view of a semiconductor device explaining a method for planarization of the semiconductor device according to the conventional art; and

Figs. 2A to 2E are cross-sectional views of a semiconductor device explaining a method for planarization of the semiconductor device to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Fig. 2A, a field oxide 11 is formed by thermally growing predetermined portions of a silicon wafer 10. Afterwards, gate oxide 12 is deposited on the wafer 10 to a thickness of 100 to 200 Å and a polysilicon layer 13 containing dopants is then deposited on the gate oxide 12 by a chemical vapor deposition. Next, a photo-mask pattern(not shown) is formed on the polysilicon layer 13 using a conventional photo-lithography method, and a gate electrode 14 is then formed by patterning the polysilicon layer 13 and the underlying gate oxide 12 using the photo-mask pattern. Impurity-doped regions 15 are formed at both sides of the gate electrode 14 in the wafer 10 using ion implantation method. Spacers 16 are provided at both side walls of the gate electrode 14 for the formation of a metal oxide semiconductor field effect transistor(MOSFET) having lightly doped drain (LDD) structure, where the spacers 16 are formed by anisotropic etching of silicon dioxide layer deposited on MOSFET structure of Fig. 2A.

Referring to Fig. 2B, an insulating layer 17 such as silicon dioxide layer is formed on whole surface of the resultant structure of Fig. 2A using a chemical vapor deposition. Afterwards, an oxide layer containing dopants, for example, a BPSG layer 18, is deposited on the insulating layer 17 at a deposition condition of atmospheric pressure and a temperature range of 400-450°C using APCVD method. It is possible to form the BPSG layer 18 using PECVD method. In this case, the BPSG layer 18 contains a high

concentration of boron and phosphorous ions. Afterwards, the wafer 10 is loaded to a reactor chamber for low pressure chemical vapor deposition(LPCVD) whose inner pressure is maintained at 10-100 mTorr, and a first thermal annealing process is performed for approximately 60 minutes.

Referring to Fig. 2C, during the first thermal annealing, boron and phosphorous ions contained in the BPSG layer 18 are diffused outwards from the surface of the BPSG layer 18, and thereby surface concentration of the BPSG layer 18 is decreased. Diffused boron and phosphorous atoms are eliminated through an outlet from the reactor chamber to the outside of the chamber by a pumping process.

Afterwards, the temperature of the reactor chamber rises to 850-900°C, and the inside of the reactor is maintained at nitrogen atmosphere. Under the above-mentioned condition, a second thermal annealing process is performed for 20-40 minutes.

As a result, the BPSG layer 18 is flowed as shown in Fig. 2D, resulting in the planarization of the surface of the wafer 10 without the precipitation of dopants taking place.

Referring to Fig. 2E, in order to form a passivation layer 19 on BPSG layer 18, N_2O gas is supplied to the reactor chamber, and a thermal oxide is formed on BPSG layer 18 by a flow process and thermal oxidation at the same temperature. In the possible case that dopants precipitate from BPSG layer 18 due to the abrupt temperature change, the passivation layer 19 made of the thermal oxde acts to prevent the generation of crystal defects when the

wafer is unloaded from the reactor chamber.

After the formation of the passivation layer 19 is completed, the temperature of the reactor chamber for LPCVD lowers to 680-720 °C, and then the wafer 10 is unloaded from the reactor chamber. At this time, the first annealing process, the second annealing process and the passivation layer forming process are performed in the same reactor chamber without vacuum break.

As described in the above, the present invention facilitates the formation of a pattern that is formed during a process subsequent to a formation process of BPSG layer but also provides superior insulating property.

Other features, advantages and embodiments of the invention disclosed herein will be readily apparent to those exercising ordinary skill after reading the foregoing disclosures. In this regard, while specific embodiments of the invention have been described in considerable detail, variations and modifications of these embodiments can be effected without departing from the spirit and scope of the invention as described and claimed.

WHAT IS CLAIMED IS:

1. A method for the planarization of a semiconductor device comprising the steps of:

providing a semiconductor substrate on which a patterned layer having topology is formed;

forming an interlevel insulating layer on the semiconductor substrate;

forming a layer for the planarization containing a dopant on the interlevel insulating layer;

diffusing the dopant contained in the layer for the planarization, outwards from the surface of the layer; and

flowing the layer for the planarization.

2. The method in accordance with claim 1, wherein said layer for the planarization is BPSG.

3. The method in accordance with claim 1, wherein diffusion of dopants is performed by a thermal annealing process.

4. The method in accordance with claim 1, wherein said diffusion step is performed for 50-70 minutes at a temperature of 650-750°C, and a pressure of 10-100 mTorr.

5. The method in accordance with claim 1, wherein said flowing step is performed for 25-35 minutes at a temperature of 850-900°C.

6. The method in accordance with claim 1, wherein both of said diffusing step and said flowing step are performed in the same chamber without vacuum break.

7. The method in accordance with claim 6, wherein both said steps are performed in LPCVD chamber.

8. The method in accordance with claim 1, further comprising the step of forming a passivation layer on the flowed layer for the planarization.

9. The method in accordance with claim 8, wherein said passivation layer is formed by a thermal oxidation process.

10. The method in accordance with claim 8, wherein said thermal oxidation process is performed at an atmosphere of N_2O.

11. The method in accordance with claim 8, wherein all of said diffusing step, said flowing step and said forming step of said passivation layer are performed in the same chamber without vacuum break.

12. The method in accordance with claim 6, wherein all said steps are performed in LPCVD chamber.

The Patent Office

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Application N : GB 9624132.8 **Examiner:** Martyn Dixon
Claims searched: all **Date of search:** 30 January 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1K (KJAP)

Int Cl (Ed.6): H01L

Other: online: WPI,JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0519393 A	(Semiconductor Process Laboratory) see especially col 2, lines 31-37, col 7, lines 14 et seq and col 8, lines 50 et seq	1-3 at least
A	US 5268333 A	(Samsung) see col 3, lines 8-12	1

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.